USB930HxADBD Adapter Board User's Manual

April 1997

Copies of documents which have an ordering number and are referenced in this document, or other Intel literature, may be obtained from:

Intel Corporation
P.O. Box 7641
Mt. Prospect, IL 60056-7641

or call 1-800-879-4683

CONTENTS

FIGURES

1.0 INTRODUCTION

This manual describes how to connect the USB930HxADBD daughter card to the 8x930 Family USB Evaluation Board Rev B. The 8x930Hx chip supports one upstream USB port and four downstream USB ports.

NOTE

Due to pin incompatibilities, this daughter card can be used with the four-port 8x930 Family USB Evaluation Board Rev B only.

2.0 INSTALLATION

2.1 Installing the Adapter Board

1. Remove the 8x930Ax device installed on the 8x930 Family USB Evaluation Board Rev B from the U3 socket prior to installing the adapter board. Refer to Figure 1 for the location of socket U3
2. Place the adapter on the evaluation board, ensuring that the connectors are properly aligned, and press the adapter onto the evaluation board until the connectors are fully engaged. Refer to Figure 2 for the correct orientation for the adapter board.

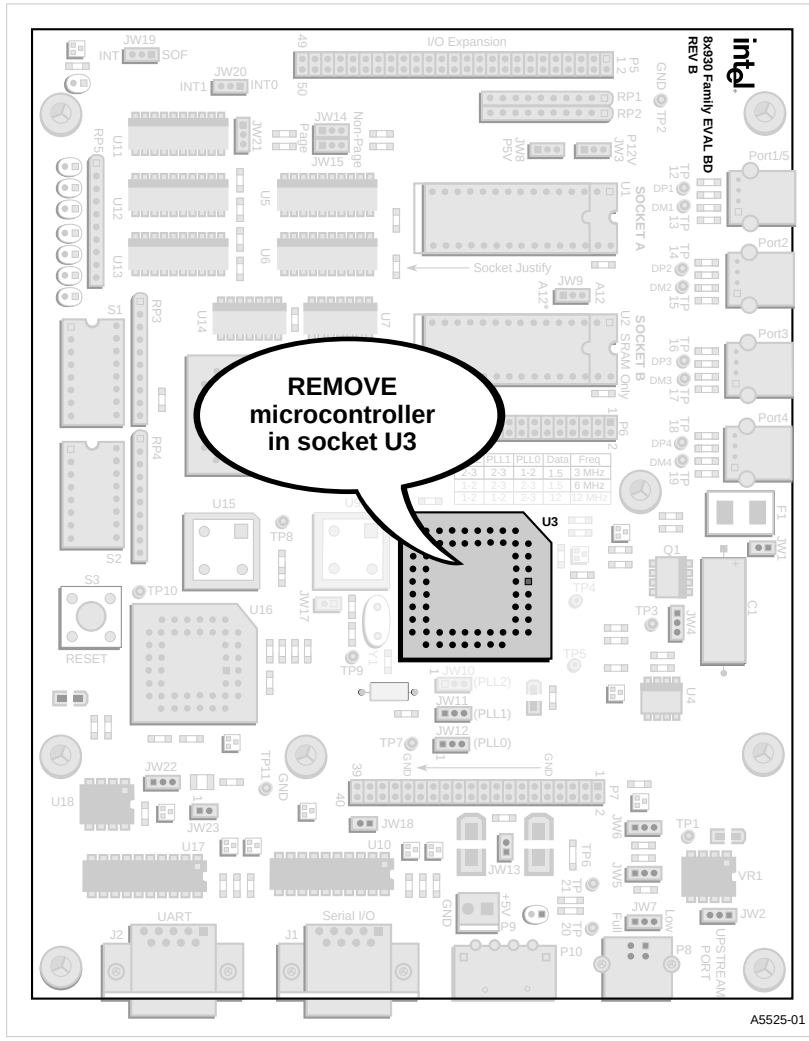


Figure 1. 8x930 Microcontroller Location

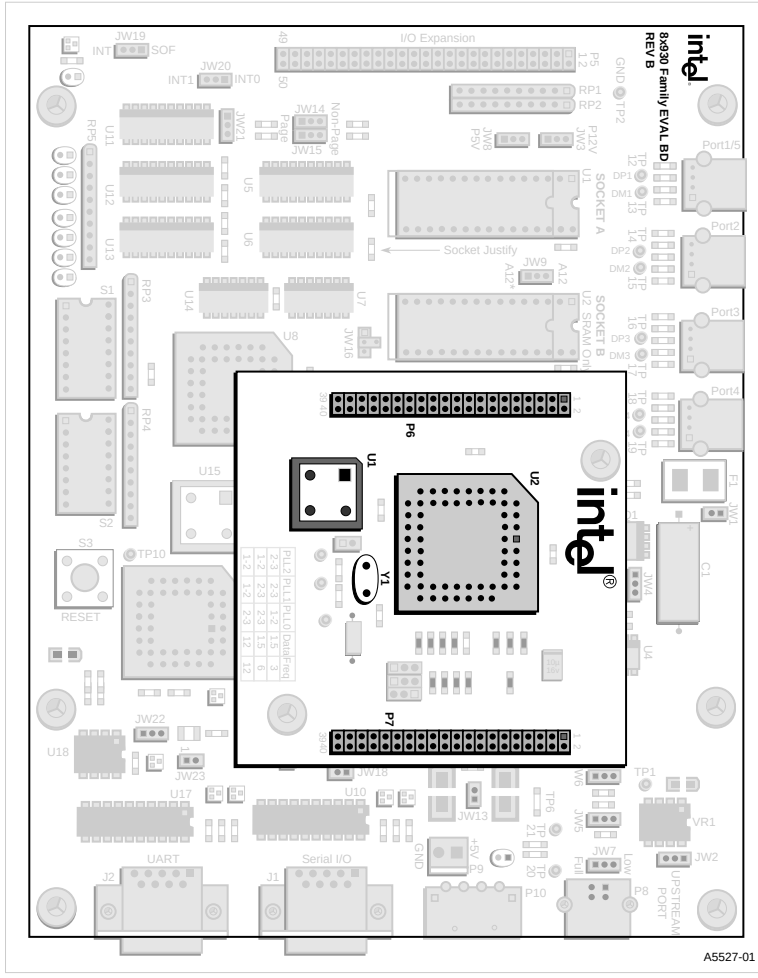


Figure 2. Adapter Board Orientation

2.2 Installing the new EPROM

If an EPROM is included in the upgrade package, you must use it to replace the EPROM that is installed in Socket A of the evaluation board. This upgraded EPROM has the same pinout as the original, however, it contains new RISM (Reduced Instruction Set Monitor) code. No jumper changes are required.

NOTE

Socket A can accept either a 32K, 64K, or 128K EPROM. Because of this, when you install the 32K EPROM provided by Intel there will be four holes left open by the notch. See Figure 3 for the correct orientation of the EPROM.

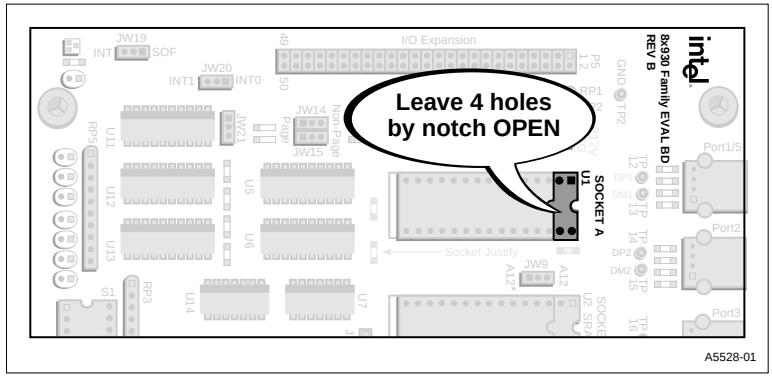


Figure 3. EPROM Orientation

3.0 BOARD LAYOUT

Figure 4 shows the layout of the board and the major components.

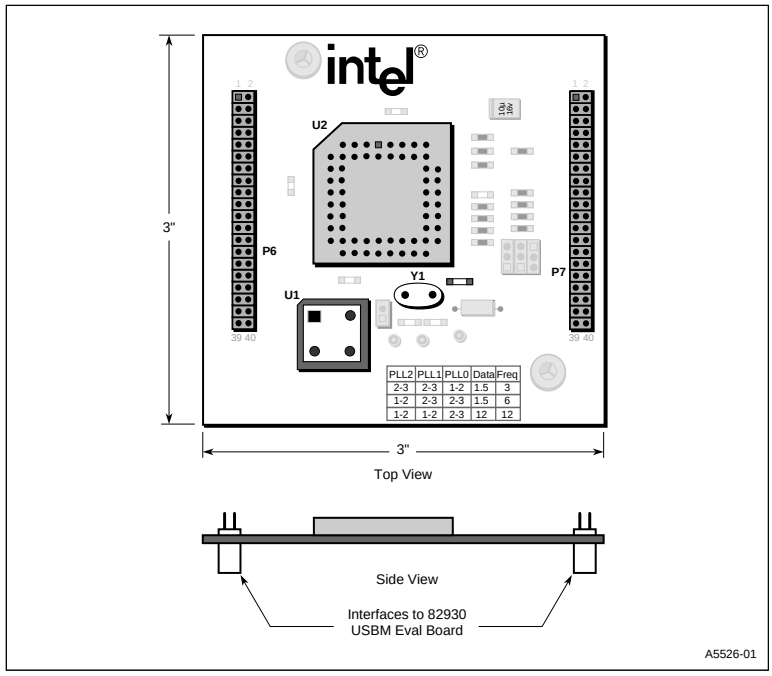


Figure 4. Adapter Board Layout

4.0 FEATURES

4.1 CPU Foot Print

The Adapter Board has the foot print for a 68-pin PLCC socket to match the pinout of the 8x930Hx.

4.2 External Clock Oscillator/Crystal

The board provides space for a crystal and a capacitor to use the internal oscillator of the 8x930Hx and also contains a clock oscillator that produces an independent external clock source for the 8x930Hx. Only one clock source can be used at a time. By default the clock oscillator is used and the crystal and capacitor are not populated. To use the internal oscillator, you must cut Jumper JW1 and install the appropriate crystal and capacitor.

4.3 Test Points

The board contains test points for CLK12MHZ, XTAL2, and AVCC.

4.4 Jumpers

The board contains jumpers to allow the 8x930Hx device to be reconfigured. Three 3-pin jumpers are used to select the core operating frequency and the USB data rate. Figure 1 illustrates jumper configurations:

Table 1. Jumper Configuration

PLL2 JW4	PLL1 JW3	PLL0 JW2	USB Data Rate	Core Frequency	XTAL1
2-3	2-3	1-2	1.5 Mbps	3 MHz	6 MHz
1-2	2-3	2-3	1.5 Mbps	6 MHz	12 MHz
1-2	1-2	2-3	12 Mbps	12 MHz	12 MHz

JW1 allows the clock oscillator to be disconnected from the 8x930Hx so that a crystal can be used. To install your own crystal, you must either cut JW1 or remove the existing clock oscillator.

NOTE

When selecting 1.5Mbps with a 3MHz core, a 6MHz crystal must be installed on the board.

4.5 Evaluation Board Interface

The 8x930Hx Adapter Board interfaces to the 8x930 Family Evaluation. Board. Rev B through two 40-pin female headers. The headers are surface mounted on the solder side of the board. The interface is "duplicated" physically and electrically on the component side of the board to allow probing access.

4.6 Serial Communications

The adapter board contains the new 8x930Hx USB chip. This device has a default start-up internal frequency of 3 MHz. You can change this frequency to 12 MHz by clearing the LC bit located in the PCON register. You can switch back to 3 MHz by setting the LC bit. Readers are encouraged to consult the *8x930Ax, 8x930Hx Universal Serial Bus Microcontroller User's Manual* (order number 272949) for more information on this subject.

The flexibility of frequency changes for power saving has a direct impact on baud rate and serial communication. To allow debugging sessions without risk of board-PC communication loss, a number of changes have been added to the RISM code. To establish communication between the evaluation board and the debugger (Keil, PLC, or Tasking software) use either the external serial link (recommended) or the internal serial link.

4.6.1 Using the External Serial Port

You are encouraged strongly to use the external serial port to communicate with the debugger environment. When this serial port is used, the baud rate is 19200 (make sure you set the debugger software to use the same rate) and all internal timers are available. The internal serial port is then free and can be used by your application. One interrupt (intr0), however, is used by the UART and cannot be used. The priority should not be changed.

The external serial port is labeled "UART" on the board To enable this port, set the UARTC switch to the "ON" position.

When using this port, you can set or clear the LC bit using the SETB and CLR instructions. There are no restrictions to your code.

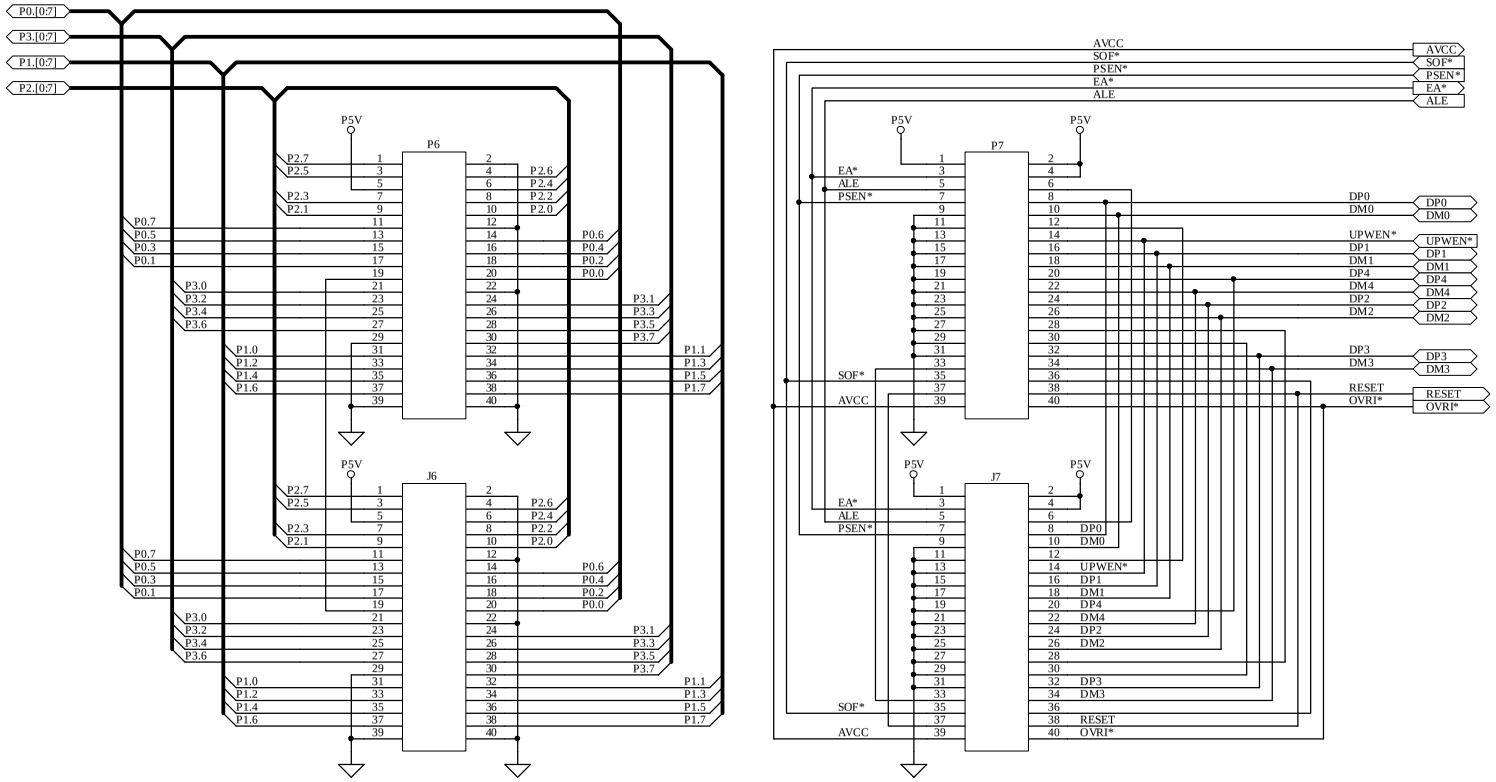
4.6.2 Using the Internal Serial Port

The use of the internal serial port to communicate with the debugger is not recommended. When you use this serial port, the baud rate is fixed at 9600 (you must set the debugger software to use the same rate) and timer-two is used by the RISM to generate the baud rate, making this timer unavailable for your application. The internal serial port is no longer available since it used to communicate with the debugger. Do not change the interrupt priority. The external interrupts, intr0 and intr1, are both available.

When using this port, you can still set or clear the LC bit. However, you cannot use the SETB and CLR instructions to do. So you must use an extended call to a routine inside the RISM that sets or clears the bit. Instead of using "SETB LC" you must use "ECALL 0FF0083" and instead of using "CLR LC" use "ECALL 0FF008B".

5.0 8X930XX ADAPTER BOARD SCHEMATICS

The pages that follow provide you with schematics for the adapter board. These files are also available on the Intel World-Wide Web sit at **`www.intel.com`**.



Although Intel has verified this design to be functional, Intel assumes no responsibility for any errors which may appear in the design. Intel reserves the right to modify this design without notice.

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USB930HxADBD Adapter Bd.

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B		0001	A

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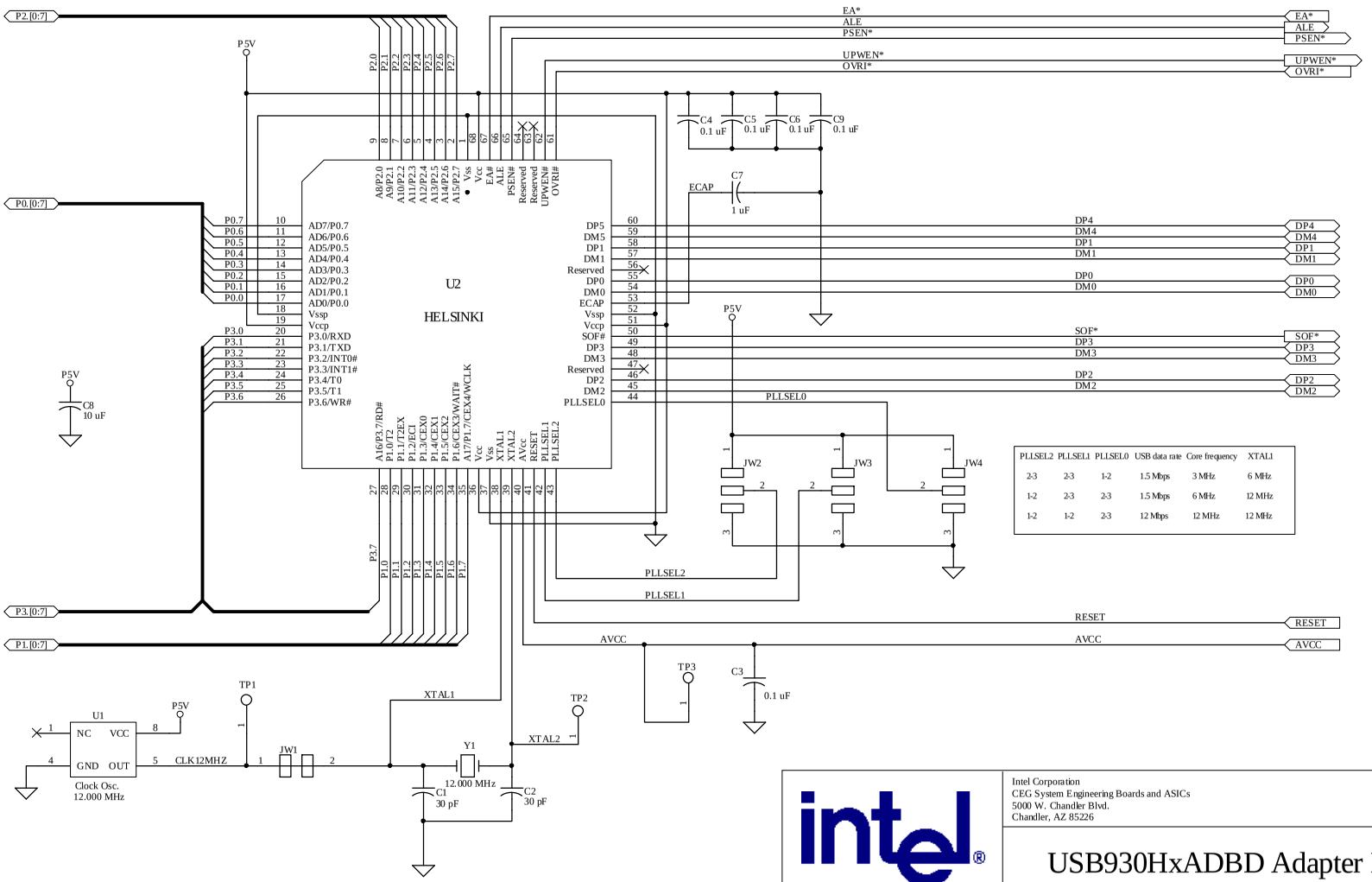

PLLSEL2	PLLSEL1	PLLSEL0	USB data rate	Core frequency	XTAL1
2-3	2-3	1-2	1.5 Mbps	3 MHz	6 MHz
1-2	2-3	2-3	1.5 Mbps	6 MHz	12 MHz
1-2	1-2	2-3	12 Mbps	12 MHz	12 MHz

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